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#### What is claimed is:

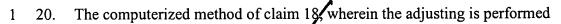
- 1 1. A computerized method of creating a layout for a circuit design, the method
- 2 comprising:
- 3 receiving a circuit design;
- 4 receiving at least one layout rule based on a reliability verification constraint
- 5 for the circuit design; and
- 6 generating a layout for the circuit design through computer automated
- 7 operations wherein the layout generated satisfies the at least one layout rule based on
- 8 the reliability verification constraint received for the circuit design.
- 1 2. The computerized method of claim 1, wherein the reliability verification
- 2 constraint arises from electromigration.
- 1 3. The computerized method of claim 1, wherein the reliability verification
- 2 constraint arises from self-heat.
- 1 4. The computerized method of claim 1, wherein the at least one layout rule
- 2 defines a maximum current for a given wire width.
- 1 5. The computerized method of claim 1, wherein the circuit design is a
- 2 microprocessor circuit design.
- 1 6. The computerized method of claim 1, wherein the layout is a two-dimensional
- 2 layout comprising a plurality of overlapping rows.
- 1 7. A computer automated placement method comprising:
- 2 placing a plurality of components of an integrated circuit design in a layout for
- 3 the integrated circuit design;
- 4 analyzing the layout for reliability verification considerations;





- 5 rearranging the plurality of components to improve the reliability verification
- 6 considerations; and
- 7 repeating the analyzing and the rearranging to further improve the reliability
- 8 verification considerations.
- 1 8. The computer automated placement method of claim 7, wherein analyzing the
- 2 layout for reliability verification considerations includes analyzing for
- 3 electromigration considerations.
- 1 9. The computer automated placement method of claim 7, wherein analyzing the
- 2 layout for reliability verification considerations includes analyzing for self heat
- 3 considerations.
- 1 10. The computer automated placement method of claim 7, further comprising
- 2 analyzing the layout for other considerations selected from the group consisting of:
- 3 layout density constraints, aspect ratio constraints, and routing complexity
- 4 constraints.
- 1 11. The computer automated placement method of claim 7, wherein placing the
- 2 plurality of components is done in a two-dimensional manner with a plurality of
- 3 overlapping row\u00e4
- 1 12. The computer automated placement method of claim 7, wherein analyzing the
- 2 layout is performed by calculating an overall unidirectional current density for the
- 3 layout.
- 1 13. A computerized method of placing a plurality of components of an integrated
- 2 circuit in a layout, the method comprising:
- assigning each one of a plurality of components of an integrated circuit to one
- 4 of a plurality of clusters;

- 5 generating a layout for each one of the plurality of clusters;
- 6 placing each one of the plurality of clusters in a layout for the integrated circuit
- 7 wherein the placing is performed in a two-dimensional manner with a plurality of
- 8 overlapping rows;
- analyzing the layout for the integrated circuit using a cost function having a
- 10 reliability verification factor; and
- rearranging the layout for the integrated circuit; and
- repeating the analyzing and the rearranging until the cost function is
- 13 minimized.
- 1 14. The computerized method of claim 13, wherein the reliability verification
- 2 factor represents the effects of electromigration and self heat.
- 1 15. The computerized method of claim 13, wherein a width of each one of the
- 2 plurality of overlapping rows is a multiple of a smallest one of the plurality of
- 3 clusters.
- 1 16. The computerized method of claim 14, wherein assigning each one of the
- 2 components is performed based on a lumped gate ordering style.
- 1 17. The computerized method of claim 14, wherein assigning each one of the
- 2 components is performed based on a distributed gate ordering style.
- 1 18. The computerized method of claim 14, further comprising adjusting one or
- 2 more of the plurality of components in one of the clusters to comply with a size
- 3 constraint.
- 1 19. The computerized method of claim 18, wherein the adjusting is performed
- 2 using device-based legging.



- 2 using stack-based legging.
- 1 21. The computerized method of claim 18, wherein the adjusting is performed
- 2 using differential legging.
- 1 22. An article comprising:
- a computer-readable medium including instructions that when executed cause a
- 3 computer to:
- 4 receive a circuit design;
- 5 receive at least one layout rule based on a reliability verification constraint for
- 6 the circuit design; and
- generate a layout for the circuit design through computer automated operations
- 8 wherein the layout generated satisfies the at least one layout rule based on the
- 9 reliability verification constraint received for the circuit design.
  - 23. The article of claim 22, wherein the reliability verification constraint arises
- 2 from electromigration.
- 1 24. The article of claim 22, wherein the reliability verification constraint arises
- 2 from self-heat
  - 25. The article of claim 22, wherein the layout is generated in a two dimensional manner having a plurality of overlapping rows.
- 1 26. An article comprising:
- a computer-readable medium including instructions that when executed cause a
- 3 computer to:

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- 4 place a plurality of components of an integrated circuit design in a two-
- 5 dimensional layout for the integrated circuit design;

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analyze the layout for rehability verification considerations; and

7 rearrange the components to improve the reliability verification considerations

8 based on the analysis of the layout.

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27. The article of claim 26, wherein the reliability verification consideration arises

2 from electromigration.

1 28. The article of claim 26, wherein the reliability verification consideration arises

2 from self-heat.

1 29. A computer-readable medium having computer-executable modules

2 comprising:

a cell library to maintain a plurality of logic gates and a plurality of layout

4 rules;

3

8

9

a schematic design tool to create a schematic of an integrated circuit using the

6 plurality of gates maintained by the cell library;

a net list tool to create a net list representation of the schematic; and

a placement tool to generate a layout of the integrated circuit from the net list

representation wherein the placement tool performs a reliability verification of the

10 layout

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30. The computer-readable medium of claim 29 further comprising a routing tool

to route wires between the plurality of logic gates in the layout.

1 31. A computerized system comprising:

2 a computer-readable medium;

a processor; and

a computer-aided design program stored on the computer-readable medium and

5 executable by the processor, the computer-aided design program comprising a

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- 6 placement module to generate a layout of an intregrated circuit wherein the
- 7 placement module performs a reliability verification of the layout.